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09/986,277	11/08/2001	Hideki Takahashi	215551US2	5052

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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/986,277	Applicant(s) TAKAHASHI, HIDEKI
	Examiner Monica Lewis	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *11 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. This action is in response to the request for continued examination filed July 7, 2003.

Response to Arguments

2. Applicant's arguments with respect to claims 1-13 and 21-32 have been considered but are moot in view of the new ground(s) of rejection.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-11 and 21-31 are rejected under 35 U.S.C. 103(a) as obvious over Takahashi (U.S. Patent No. 5,960,264) in view of Majumdar et al. (U.S. Patent No. 5,623,152).

In regards to claim 1, Takahashi discloses the following:

a) a first semiconductor layer (41) of a first conductivity type having first and second major surfaces (For Example: See Figure 3);

b) a second semiconductor layer (46) of a second conductivity type formed on the first major surface of said first semiconductor layer (For Example: See Figure 3);

c) a third semiconductor layer (42) of the second conductivity type formed on said second semiconductor layer (For Example: See Figure 3);

d) a fourth semiconductor layer (43) of the first conductivity type formed on said third semiconductor layer (For Example: See Figure 3);

e) at least one first trench and at least one second trench arranged to penetrate through at least said fourth semiconductor layer from a surface of said fourth semiconductor layer such that a bottom part of an external wall of said at least one second trench is in direct contact with a region of the second conductivity type (For Example: See Figure 3);

f) a first semiconductor region (44) of the second conductivity type selectively formed in said surface of said fourth semiconductor layer vicinal to said at least one first trench (For Example: See Figure 3);

g) a first insulating film (48) formed on an internal wall of said at least one first trench (For Example: See Figure 3);

h) a first material serving as a control electrode (49) buried in at least one first trench and formed on said first insulating film (For Example: See Figure 3);

i) a first main electrode (51) electrically connected to at least a part of said first semiconductor region and formed over an almost whole surface of said fourth semiconductor layer (For Example: See Figure 3); and

j) a second main electrode (52) formed on the second major surface of said first semiconductor layer (For Example: See Figure 3).

In regards to claim 1, Takahashi fails to disclose the following:

a) a second material formed in said at least one second trench, the second material not being a control electrode.

However, Majumdar et al. ("Majumdar") discloses a second material formed in at least one second trench, the second material not being a control electrode. (For Example: See Figure 13). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Takahashi to include a second material formed in at least one second trench, the second material not being a control electrode

as disclosed in Majumdar because it aids in decreasing transient voltage (For Example: See Column 1 Lines 5-12 and Column 4 Lines 32-36).

Additionally, since Takahashi and Majumdar are both from the same field of endeavor, the purpose disclosed by Majumdar would have been recognized in the pertinent art of Takahashi.

In regards to claim 2, Takahashi discloses the following:

a) distance between said at least one first trench and said at least one second trench is set to 5 *u*m or less (For Example: See Column 17 Lines 64-66).

Additionally, the applicant has not established the critical nature of the dimension of 5 *u*m or less. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 3, Takahashi discloses the following:

a) at least one first trench includes a trench formed in a predetermined direction along said first major surface of said fourth semiconductor layer (For Example: See Figure 3);

b) one second trench includes a trench formed in said predetermined direction seen on a plane (For Example: See Figure 3);

c) first semiconductor region includes a first section formed in a vicinity of said at least one first trench and a second section extended from said first partial region in such a direction as to go away from said at least one first trench (For Example: See Figure 3); and

d) first main electrode is directly formed on said second section to carry out an electrical connection to said first semiconductor region (For Example: See Figure 3).

In regards to claim 4, Takahashi discloses the following:

a) a third section which is further extended from said second partial section and is formed in a vicinity of said at least one second trench (For Example: See Figure 3); and

b) first main electrode is further formed directly on said third section to carry out said electrical connection to said first semiconductor region (For Example: See Figure 3).

In regards to claim 5, Takahashi discloses the following:

a) second and third sections include a plurality of second and third partial regions respectively (For Example: See Figure 15 and Figure 21); and

b) plurality of third sections are selectively formed in the vicinity of said at least one second trench (For Example: See Figure 15 and Figure 21).

In regards to claim 6, Takahashi discloses the following:

a) a second semiconductor region of the first conductivity type formed in said surface of said fourth semiconductor layer contiguous to said at least one second trench, said second semiconductor region having a concentration of an impurity of the first conductivity type set to be higher than that of said fourth semiconductor layer (For Example: See Figure 3).

In regards to claim 7, Takahashi discloses the following:

a) concentration of said impurity of the first conductivity type in said second semiconductor region is set to be higher than a concentration of an impurity of the second conductivity type in said first semiconductor region (For Example: See Figure 3).

In regards to claim 8, Takahashi discloses the following:

a) a plurality of second trenches (For Example: See Figure 15).

In regards to claim 9, Takahashi discloses the following:

a) at least one first trench and said at least one second trench have equal formation widths (For Example: See Figure 3).

In regards to claim 10, Takahashi discloses the following:

a) a second insulating film formed on an internal wall of said at least one second trench (For Example: See Figure 3).

In regards to claim 11, Takahashi discloses the following:

a) conductive region buried in said at least one second trench and formed on said insulating film (For Example: See Figure 3).

In regards to claim 21, Takahashi discloses the following:

a) first semiconductor region is not vicinal to said at least one second trench (For Example: See Figure 3).

In regards to claims 22 and 23, Takahashi discloses the following:

a) the first main electrode is formed in direct contact over an entire top surface of said fourth semiconductor layer around said at least one second trench (For Example: See Figure 3).

In regards to claim 24, Takahashi discloses the following:

a) a plurality of first trenches, wherein said at least one second trench is provided between two adjacent first trenches (For Example: See Figure 3).

In regards to claim 25, Takahashi discloses the following:

a) a plurality of second trenches provided between two adjacent first trenches (For Example: See Figure 3).

In regards to claim 26, Takahashi discloses the following:

a) the first main electrode is formed in direct contact over an entire top surface of said fourth semiconductor layer among said plurality of second trenches (For Example: See Figure 3).

In regards to claim 27, Takahashi discloses the following:

a) the first main electrode is formed in direct contact over entire said top surface of said fourth semiconductor layer between each first trench of said plurality of first trenches and each second trench of said plurality of second trenches (For Example: See Figure 3).

In regards to claim 28, Takahashi discloses the following:

a) the first main electrode is formed in direct contact over an entire top surface of said fourth semiconductor layer around said at least one second trench (For Example: See Figure 3).

In regards to claim 29, Takahashi discloses the following:

a) the first main electrode is formed in direct contact over entire said top surface of said fourth semiconductor layer between each first trench of said plurality of first trenches and said at least one second trench (For Example: See Figure 3).

In regards to claim 30, Takahashi discloses the following:

a) the first main electrode is formed in direct contact over an entire top surface of said fourth semiconductor layer around said at least one second trench (For Example: See Figure 3).

In regards to claim 31, Takahashi discloses the following:

a) the first main electrode is formed in direct contact over entire said top surface of said fourth semiconductor layer between said at least one first trench and said at least one second trench (For Example: See Figure 3).

6. Claim 12 is rejected under 35 U.S.C. 103(a) as obvious over Takahashi (U.S. Patent No. 5,960,264) in view of Majumdar et al. (U.S. Patent No. 5,623,152) and Uenishi et al. (U.S. Patent No. 5,894,149).

In regards to claim 12, Takahashi fails to disclose the following:

a) first main electrode is directly formed on said conductive region.

However, Uenishi et al. ("Uenishi") discloses an electrode (10) formed on a conductive region (80) (For Example: See Figure 42). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Takahashi to include an electrode formed on a conductive region as disclosed in Uenishi because it aids reducing the area of the trenches (For Example: See Column 20 Lines 18-39).

Additionally, since Takahashi and Uenishi are both from the same field of endeavor, the purpose disclosed by Uenishi would have been recognized in the pertinent art of Takahashi.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as obvious over Takahashi (U.S. Patent No. 5,960,264) in view of Majumdar et al. (U.S. Patent No. 5,623,152) and Takahashi (U.S. Patent No. 6,001,678).

In regards to claim 13, Takahashi fails to disclose the following:

a) a sixth semiconductor layer of the second conductivity type formed between said first semiconductor layer and said second semiconductor layer, said sixth semiconductor layer having a concentration of an impurity of the second conductivity type higher than that of said second semiconductor layer.

However, Takahashi discloses a sixth layer (61) of the second conductivity type (For Example: See Figure 12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Takahashi to include a sixth layer of a second conductivity type as disclosed in Takahashi because it aids increasing the switching speed (For Example: See Column 7 Lines 39-46).

Additionally, since Takahashi and Takahashi are both from the same field of endeavor, the purpose disclosed by Takahashi would have been recognized in the pertinent art of Takahashi.

8. Claim 32 is rejected under 35 U.S.C. 103(a) as obvious over Takahashi (U.S. Patent No. 5,960,264) in view of Majumdar et al. (U.S. Patent No. 5,623,152) and Takahashi (U.S. Patent No. 5,864,159).

In regards to claim 32, Takahashi fails to disclose the following:

a) first material is identical to said second material.

However, Takahashi discloses a first material that is identical to the second material (For Example: See Figure 23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Takahashi to include a

first material that is identical to the second material as disclosed in Takahashi because it aids in improving the breakdown voltage (For Example: See Column 9 Lines 26-39).

Additionally, since Takahashi and Takahashi are both from the same field of endeavor, the purpose disclosed by Takahashi would have been recognized in the pertinent art of Takahashi.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
September 23, 2003

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